IN THE SPECIFICATION

Please amend paragraph [0019] as follows:

In accordance with the present invention, a PLL circuit is disclosed that includes a VCO having a resonant circuit with a plurality of individually selectable capacitive elements corresponding to various ~~having~~ different tuning ranges, and including a control circuit that selects one of the tuning ranges in response to either externally generated or internally generated control signals. In the following description, exemplary embodiments are described in order to provide a thorough understanding of the present invention. For purposes of explanation, specific nomenclature is set forth to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details may not be required to practice the present invention. In other instances, well-known circuits and devices are shown in block diagram form to avoid obscuring the present invention unnecessarily. Additionally, the interconnection between circuit elements or blocks may be shown as buses or as single signal lines. Each of the buses may alternatively be a single signal line, and each of the single signal lines may alternatively be a bus. Further, the logic states of various signals described herein are exemplary and therefore may be reversed or otherwise modified as generally known in the art. Accordingly, the present invention is not to be construed as limited to specific examples described herein but rather includes within its scope all embodiments defined by the appended claims.

Please amend paragraph [0041] as follows:

MUX 608, which is well-known, includes a first input to receive CNT[0,1] from counter 606, a second input to receive the 2-bit mode signal MS[0,1], an output to provide control signals ~~GS[0,1]~~ GC[0,1] to decoder 612, and a control terminal coupled

to an output of logic gate 610, which includes an input to receive the mode select signal MS[0,1]. Referring also to FIG. 7, for one embodiment, logic gate 610 is an OR gate 702 having inputs to receive MS[0] and MS[1] and an output to provide a select signal SEL to MUX 608. In this manner, if both MS[0] and MS[1] are logic low, OR gate 702 provides a logic low SEL to MUX 608, which in turn provides the signal CNT[0,1] from counter 606 as the control signal GC[0,1] to decoder 612. Conversely, if either MS[0] or MS[1] is logic high, OR gate 702 provides a logic high SEL to MUX 608, which in turn provides the mode select bits MS[0,1] as GC[0,1] to decoder 612.